

High Yield, Single Droplet Electrode Arrays for Nanoscale Printed Electronics

Mario Caironi,* Enrico Gili, Tomo Sakanoue, Xiaoyang Cheng, and Henning Sirringhaus*

Cavendish Laboratory, JJ Thomson Avenue, Cambridge, CB3 0HE, United Kingdom

As the range of nanoscale electronic materials is rapidly expanding, there is a growing need for scalable patterning techniques that allow probing of the electronic properties of materials such as carbon nanotubes,^{1–3} graphene,^{4,5} nanowires,^{6,7} or organic semiconductors^{8,9} on a typical length scale of 100 nm. Traditionally, techniques such as electron beam lithography¹⁰ or nanoimprinting¹¹ are used to define suitable electrode structures.

While these techniques are capable of exceptionally high resolution and high patterning yield on flat, rigid substrates such as silicon wafers, they are less well suited to nonplanar, stretchable and/or flexible substrates. There is a growing interest in using direct-write, solution-based printing techniques¹² for electrode fabrication on such substrates. Additive printing offers advantages in terms of process simplification, layer-to-layer alignment, compatibility with large-area processing, and potential cost reduction compared to subtractive lithographic patterning. However, there are only a few examples of printing techniques that are capable of achieving sufficiently high resolution for definition of electrode gaps on a 100 nm scale.^{13,14} For conventional graphic arts printing techniques such as inkjet printing,¹⁵ resolution as well as patterning yield is limited by the relative large ink volume deposited in each droplet onto the substrate (1 pL corresponds to a droplet diameter of 12 μm) and the poor control of ink spreading on the substrate. The issue of droplet volume has been addressed by developing special electrohydrodynamic-jet printers^{16,17} capable of delivering subfemtoliter ink volumes. This allows definition of channel lengths down to 1 μm,¹⁸ coming, however,

ABSTRACT In this work we demonstrate two building blocks of a scalable manufacturing technology for nanoscale electronic devices based on direct-write printing: an architecture for high-yield printing of electrode gaps with 100 nm dimension and a low-temperature silver complex ink for integration of organic materials with high conductivity metal interconnects. We use single printed droplets that are made to dewet slowly from each other to allow reliable, high yield patterning even in the presence of certain surface defects.

KEYWORDS: inkjet printing · organic field-effect transistor · self-aligned printing · submicrometer channel · printed contact array · printed electronics · high resolution printing

at the cost of reduced throughput. An alternative is the recently developed self-aligned printing (SAP) technique, which is capable of 100 nm resolution in a bottom-up process while preserving the throughput of commercial drop-on-demand (DOD) printing systems^{14,19} and allows achieving fast-switching printed organic transistors with transition frequencies of 1.6 MHz.²⁰

Whether such high resolution printing techniques will become widespread tools for applications in nanoelectronics on the 100 nm length scale will depend much on what patterning yield and uniformity will be achievable. It is fair to say that at present there is considerable skepticism whether a solution-based printing technique would be capable of defining large electrode arrays with gaps on the 100 nm scale without electrical shorts. A closely related, important requirement is that the metallic inks would need to offer conductivities close to those of bulk metals such as copper or silver in order to reduce parasitic voltage drops along long printed electrodes and interconnects. Such metallic conductivities would have to be achieved at low process temperatures (<150 °C) to be compatible with plastic substrates and, particularly, with the limited temperature stability of molecular

*Address correspondence to
hs220@cam.ac.uk,
mc582@cam.ac.uk.

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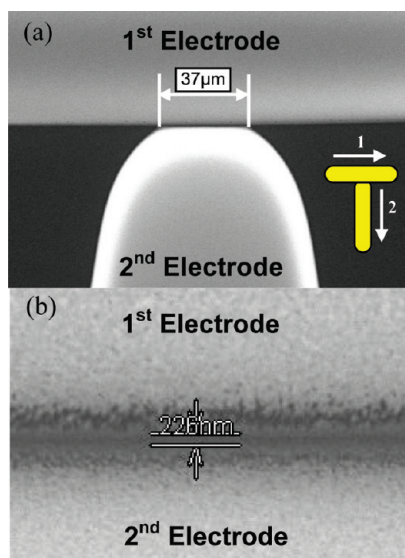


Figure 1. SEM images of “T-shaped” SAP gold electrodes, where the second contact is printed at an angle of 90° with respect to the first one and the channel width is defined by a single droplet. The naturally rounded shape of the droplet conforms to the edge of the first electrode and is deformed into a straight line along the edge of the first contact (a). In this region a submicrometer electrically insulating gap is created. This is magnified in panel b, where a clear gap of ~ 200 nm can be observed.

electronic materials. In the present work we aim to address both challenges.

The SAP technique is based on printing a first conductive electrode line, modifying its surface with a self-assembled monolayer (SAM) to become repulsive to the ink, and then printing a second conductive electrode line along the edge of the first electrode, such that the ink droplets flow off the first conductive electrode and dry in close proximity to, but not in electrical contact with, the first printed electrode. In between the two printed electrodes a small gap of 200–400 nm is formed. In our previous work we used a standard electrode configuration in which the two linear-shaped electrodes printed from multiple droplets run parallel to each other over several hundred micrometers. In this device configuration we find that the yield is moderate and a significant number of devices is shorted.^{14,19} Here, we report on a new configuration based on single droplet contacts which, by favoring a better understanding and control of the SAP process, allows the achievement of a surprisingly high device yield of 94–100% on arrays with very low leakage currents. We also demonstrate the use of a low-temperature silver complex precursor ink that can be integrated with underlying organic semiconductors and dielectrics to provide interconnects and electrodes with near bulk silver conductivities at 130°C .

RESULTS AND DISCUSSION

In Figure 1 SEM images of the SAP gold contacts are shown. The first contact is inkjet printed in a line

shape on a glass substrate from a gold-nanoparticles-based ink (Harima). After sintering, its surface is subsequently modified with a SAM of *1H,1H,2H,2H*-perfluoro-1-decanethiol (PFDT). The perfluorinated SAM selectively deposited on the first contact strongly reduces its surface energy, thus creating, with respect to the hydrophilic glass substrate, a surface energy contrast that enables the SAP technique.^{14,19} The second contact is printed at an angle of 90° with respect to the first one, realizing a characteristic “T-shape” (inset of Figure 1a). The length and shape of the two “arms” can be chosen to allow suitable interconnections, but, importantly, the channel width (W) is defined by a single droplet only. The droplet that comes in contact with the first electrode is made to dewet off the surface of the first electrode by the PFDT surface coating and conforms to the edge of the first electrode. Its naturally rounded shape is deformed into a straight line along the edge of the first contact. In this region a submicrometer electrically insulating gap is created, yielding a channel width of a few tens of micrometers (Figure 1a), mainly depending on the spreading of the ink on the substrate. A typical channel, as it appears after sintering of the second contact, is magnified in Figure 1b, where a clear gap of ~ 200 nm can be observed.

The T-shaped single droplet electrode configuration has been found to be critical to achieve high yields for forming electrically insulating electrode gaps without shorts. The reason is that in the T-shaped architecture the channel formation is determined by the fluid dynamics and dewetting of a single droplet only and allows easier optimization than for two parallel printed electrode lines as used in previous work.^{19,20} For the latter, dewetting of each droplet is also affected by the state of previously and subsequently deposited droplets. The effect of subsequently deposited droplets is, for example, to hinder the dewetting of a particular droplet because of it being pulled back by subsequent droplets that are being printed overlapping with the first electrode. In terms of failure analysis there is the additional benefit that for a single droplet channels it is practical to observe the entire channel with SEM and correlate the occurrence of any electrical leakage current in defective devices with specific defects along the edge of the channel.

To achieve high yield, a second critical factor apart from device configuration is the drying time of the ink. By using high boiling solvents and allowing several minutes for slow drying at room temperature before the high temperature sintering step, the ink for the second contact will eventually dewet with very high yield. A series of optical microscopy images are reported in Figure 2, where it is possible to follow the complete dewetting from the first electrode over a period of 6 min after printing. We observe that 60 s after printing a portion of the second electrode still overlaps with the first

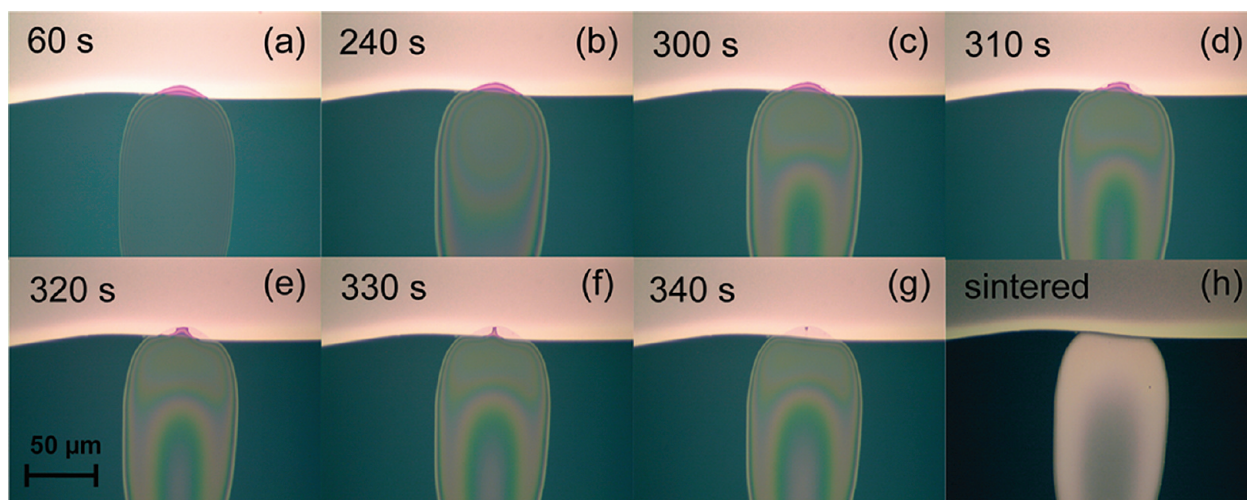


Figure 2. Optical microscope images illustrating the temporal evolution of the complete dewetting of a line which shows overlap with the first pattern $t = 60$ s (a) after printing. For $t \leq 240$ s substantially no variations can be observed (b), while for $t \geq 300$ s, together with a variation of the ink color due to partial evaporation of the dispersing solvents, the contact line retracts. The dewetting process is complete only after 340 s (c–g). Upon sintering of the second line (h), the SAP electrodes are reliably formed.

electrode (Figure 2a). No significant evolution can be observed over the next 3 min (Figure 2b and Supporting Information, Figure S1). Subjecting the sample to the sintering temperature of 250 °C at this time would induce a fast drying of the ink and lead to a significant number of short circuits. If the ink is left to dry at room temperature for longer, complete dewetting from the first line occurs in a very reliable manner on a time scale of 5–7 min. Under such slow drying conditions dewetting is even tolerant to surface defects. It can be seen that after 310 s (Figure 2d) the contact line starts to dewet from the surface of the first electrode in some regions but remains pinned in others, presumably as a result of local surface defects on the first electrode. At 340 s (Figure 2g) the contact line has completely depinned from these defects. Dewetting is now complete, and sintering at this stage results in reliable formation of a nanochannel (Figure 2h). We observe some color contrast in the optical microscopy images on the first electrode from where the droplets have dewetted (Figure 2g). This is either due to interactions of the ink solvent with the surface of the first electrode or due to some solvent/nanoparticle residues left after dewetting. However, this contrast disappears after sintering and does not appear to have any impact on the yield of nanochannel formation. We can follow the continuous drying of the ink through the observation of interference fringes and colors across the second printed line. This interference contrast continues to change over the period of 6 min. The slow evaporation of the solvent exerts a sufficiently strong force on the contact line to pull the pinned contact line back from the surface of the first electrode reliably, even when certain surface defects are present.

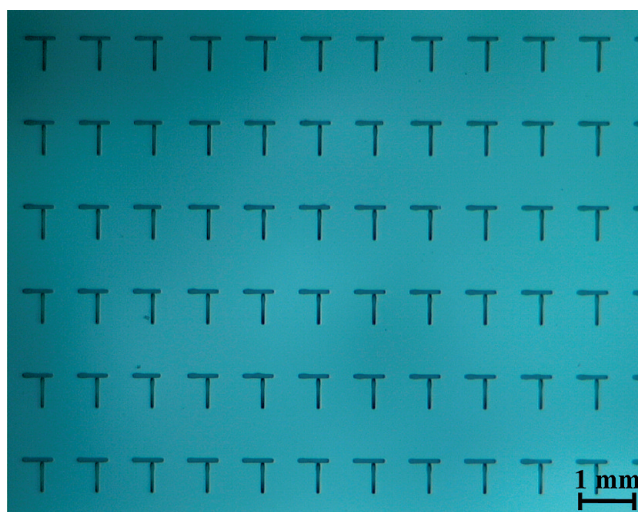


Figure 3. Optical microscope image (transmission) showing part of one of the 6×12 arrays of SAP contacts fabricated, where 6 rows and 11 columns can be seen.

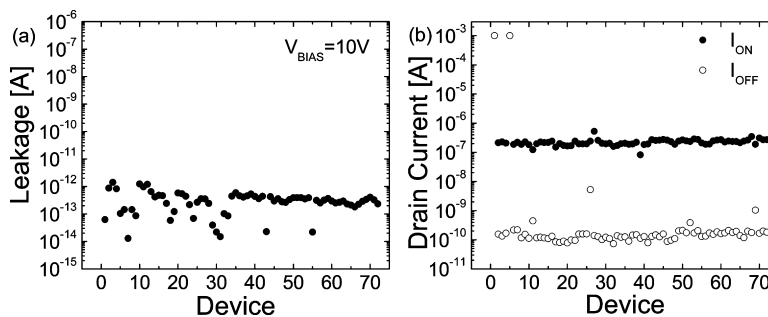


Figure 4. (a) Yield measurement on a 6×12 array of single-droplet SAP gold electrodes. The leakage current in air, at an applied voltage of 10 V across the submicrometer gaps, is plotted for each device. None of the 72 devices shows a leakage higher than 2 pA. (b) ON drain currents I_{ON} (extracted at an applied drain bias voltage V_D of -1 V and gate voltage V_G of -10 V) and OFF drain currents I_{OFF} ($V_D = -1$ V, $V_G = +5$ V) of a 6×12 array of TIPS-pentacene SAP FET with a ~ 130 nm thick CYTOP dielectric. Only two devices are shorted and the yield is higher than 97%. Assuming $L = 400$ nm and $W = 40$ μm , an average saturated field-effect mobility ~ 0.03 $\text{cm}^2/(\text{V s})$ is extracted.

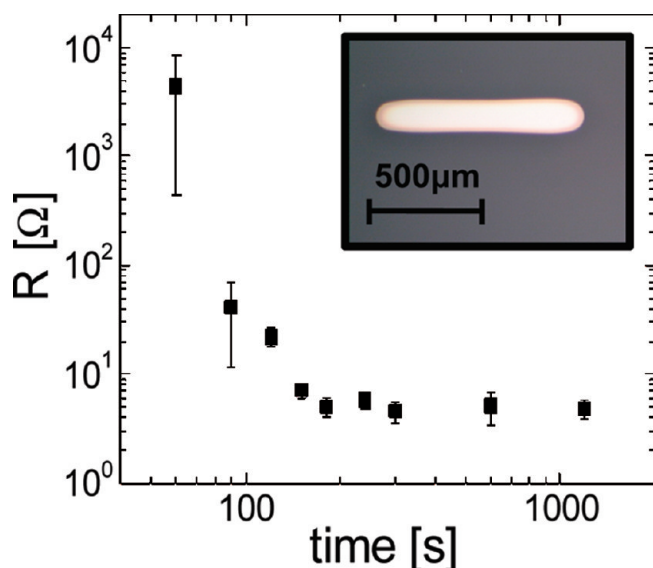


Figure 5. Dependence of the resistance of a $\sim 700 \mu\text{m}$ long Ag-complex (TEC-IJ-010) printed line on PMMA on the sintering time. The annealing was performed at 130°C in ambient air. After 2–3 min a resistivity of only a few times $10^{-6} \Omega\text{cm}$ is reached. A typical line printed with a $30 \mu\text{m}$ nozzle at 1 kHz and sintered for 5 min is shown in the inset.

To assess the reliability of the reported printing process for the realization of submicrometer contacts we have fabricated 6×12 test arrays. In Figure 3 an optical microscope image of one of such arrays is shown, where the printing uniformity of the T structures can be

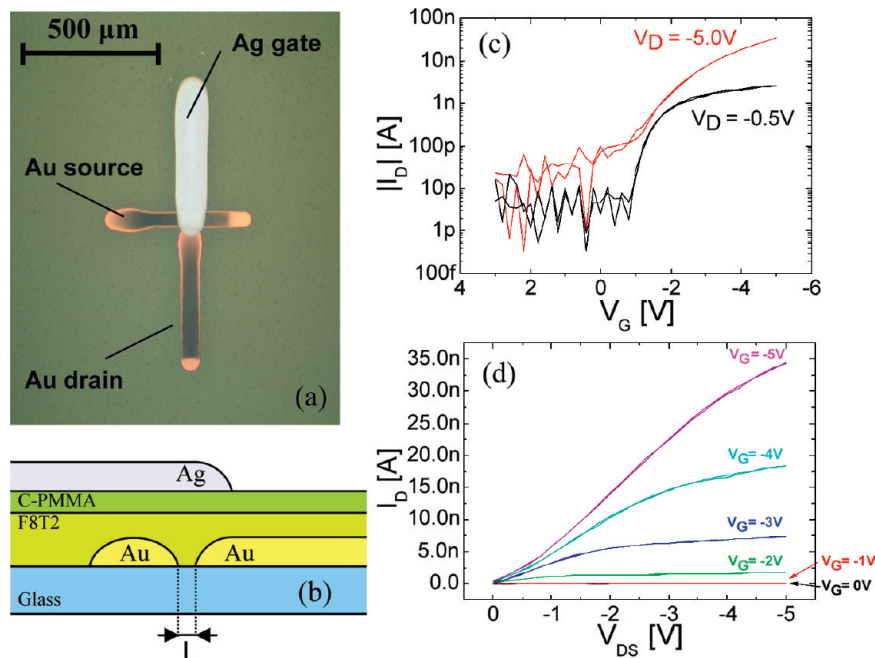


Figure 6. (a) Optical microscopy image of a complete and functional transistor, where the gold SAP source and drain contacts in the T-shaped configuration and the silver gate contact can be seen. (b) Schematic cross-sectional diagram of the top-gate device architecture: on top of the SAP gold electrodes F8T2 polymer semiconductor and C-PMMA gate dielectric layers are deposited by spin-coating. On top of the cross-linked dielectric, a silver gate line is printed and sintered. (c) Transfer and (d) output characteristic curves of the device shown in panel a with $L \approx 200 \text{ nm}$ and a gate dielectric thickness of $\sim 50 \text{ nm}$; both forward and reverse scans are plotted. Clean saturation at voltages as low as a few volts and an ON/OFF ratio of $10^3 - 10^4$ are observed. The OFF current in the pA range is limited by gate leakage currents and not by the even lower leakage current between the SAP electrodes (100 fA) as measured in Figure 4.

appreciated on a macroscopic scale. In Figure 4a we report the yield and leakage currents of an array at an applied bias of 10 V: all 72 contacts show a leakage current lower than 2 pA, close to the detection limit of our measurement setup. Breakdown voltages higher than 2 MV cm^{-1} were measured. On some arrays (Supporting Information, Figure S2 – S4) we observed a few devices with higher leakage currents. These channels are typically associated with clearly visible particle defects in the channel region (Supporting Information, Figure S3). By improving the substrate and general cleanliness of the process, it should be possible to eliminate such residual defects. Note that even in such cases devices do not short electrically but merely exhibit nanoampere leakage currents.

Another important aspect to assess is the variation across the electrode arrays of the gaps width W and length L . To provide an indirect measurement of the spreading of such parameters, we measured the ON and OFF drain currents, which are proportional to W/L ,²¹ of field-effect transistors (FETs) fabricated using the SAP electrodes as source and drain contacts (Supporting Information, Figure S5). The device architecture of choice is a top-gate, staggered one in order to take advantage of lower contact resistance.²² For these test devices, whose main purpose is to monitor the distribution of the currents, we adopted a uniform 6,13-

bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene)²³ layer, spun from a low boiling point solvent, as the semiconductor and a $\sim 130 \text{ nm}$ thick perfluorinated polymer, known with the commercial name of CYTOP,²⁴ as the dielectric. In Figure 4b the ON and OFF drain currents for all the 72 devices in an array, with $W \approx 40 \mu\text{m}$ and $L \approx 400 \text{ nm}$ on average, are shown. If we exclude the two shorted devices, the ON current is quite uniform across the entire array, with a mean value of 223 nA and a standard deviation (σ) of 57 nA (Supporting Information, Figure S6). Correspondingly the ON/OFF ratio (Figure S6c) has a mean value of 1.6×10^3 and $\sigma = 0.6 \times 10^3$, where σ is mainly limited by a small number of electrodes showing a higher source-drain leakage (Figure S6b). These results support a limited variability of W and L across the array and the good reliability of the proposed process.

Finally we address the integration of a printable top metal contact, needed in FETs, and generally in any integrated device structures, where it is necessary to have at least two levels of printed metallization. To replace the

commonly thermally evaporated electrode, for the top-level metallization (gate-level) we use the silver complex ink TEC-IJ-010 (InkTec Co., Ltd.) which can be converted into a highly conducting electrode at low temperatures to avoid degradation of the underlying organic semiconductor and dielectric layers. After only 3 min at 130 °C in ambient air, the sintering process is complete and the lines show a resistance of a few ohms (see Figure 5), corresponding to an estimated resistivity in the range of $(5-10) \times 10^{-8} \Omega\text{m}$, close to the silver bulk resistivity of $1.587 \times 10^{-8} \Omega\text{m}$. A similar printed line of a commonly used PEDOT:PSS based ink (H.C. Starck) would give a resistivity a few orders of magnitude higher.²⁰ To prove the compatibility of the printed silver line with our SAP architecture in a fully solution-processed FET, we adopted a test system based on the well-known poly(9,9-dioctylfluorene-co-bithiophene) (F8T2), serving as a good reference semiconductor and a ~ 50 nm cross-linked poly(methyl methacrylate) (C-PMMA) dielectric layer,²⁵ suitable for withstanding the top electrode printing process. In Figure 6a the T-shaped gold SAP source and drain contacts together with the silver gate electrode can be seen. The device has a compact design and a minimum footprint suitable to be compatible with high density circuit integration limited only by the printed electrode line width. In Figure 6d the output characteristics of an all-printed F8T2 FET with $L \approx 200$ nm are reported. Clean saturation at voltages as low as a few volts is observed, reflecting the correct scaling of the gate dielectric thickness (~ 50 nm). The device operates at voltages lower than 5 V and has a field-effect mobility of $2 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is typical for unaligned, long-channel F8T2 transistors with PMMA gate dielectric.¹⁴ This demonstrates the compatibility of the silver complex ink and its sinter-

ing process with underlying organic semiconductor and dielectric layers.

CONCLUSIONS

We have developed a technique for fabricating arrays of metal electrode gaps with 200–500 nm dimension and high device yield by inkjet printing. The technique is based on applying the recently developed self-aligned printing technique in a single-droplet T-shaped architecture, which not only reduces the footprint of the electrode structure but also makes the ink dewetting process more robust against substrate and printing defects that could potentially create electrical shorts. Thanks to the proposed architecture it is also possible to pattern contacts arrays with good uniformity, a very important aspect for nanoscale printed electronics applications. We have also demonstrated an inkjet printable silver-complex-based ink which can be sintered at low temperatures of 130 °C to achieve near bulk silver conductivity and is fully compatible with integration with organic semiconductors and dielectrics. Thanks to this, fully solution-processed organic FETs were realized, without the use of any mask during the fabrication process.

We believe that our work provides new tools for scalable printing-based manufacturing of nanoscale electronic devices. The single-droplet printed nanoscale contacts could be applied not only to organic semiconductors, but also to other nanomaterials, such as carbon nanotubes, graphene, and inorganic nanowires, for which electrical contacts over a length scale of 100 nm are required. For such systems one could even make use of the digital patterning capability of inkjet printing to make contacts to nano-objects that are distributed irregularly on the substrate.

MATERIALS AND METHODS

As substrates we used thorough cleaned Corning 1737F glass slides. The metal ink adopted to print the T-shaped electrodes was based on Harima NPG-J gold nanopaste, diluted 1:3 by volume with xylene and filtered with a 0.2 μm PTFE filter. The printing was performed at room temperature and at a jetting frequency of 1 kHz. After printing the first electrodes, the samples were sintered on a hot plate at 250 °C for 1 h in air. PFDT for the modification of the surface energy of the first electrode was purchased from Fluorochem and used as received by immersing the samples in a 10 mM isopropyl alcohol (IPA) solution for 20 min. The samples were then rinsed in IPA and dried with a nitrogen gun, prior to printing of the second electrode from the same gold nanopaste. When fabricating FETs, before the deposition of the semiconductor layer, the contacts were modified again with pentafluoro-benzenethiol in the case of TIPS-p devices and PFDT in the case of F8T2 to improve charge injection.^{20,26} The semiconducting TIPS-pentacene was dissolved in anhydrous chloroform (10 g L^{-1}) and spun at 4000 rpm for 3 min in N_2 atmosphere. In this case the solution was deposited with the substrates already rotating. Here we are interested in the spreading of the FETs currents, rather than obtaining the highest possible mobility and therefore TIPS-pentacene was deposited on top of the nanochannel electrodes by spin-coating from a low boiling point solvent, forming an amorphous and uni-

form film, with a very smooth surface across the entire array. This was done to reduce possible variations in the device parameters due to morphological differences in the semiconductor and to minimize the creation of pinholes through the thin gate dielectric. On top of the semiconductor a CYTOP dielectric layer was deposited by spin-coating at 500 rpm for 10 s, followed by 90 s at 2000 rpm, a CTL-809 M solution (Asahi Glass) diluted 1:2 in volume with CT-solvent 180. An annealing at 90 °C for 30 min followed. In this case the gate contact was realized by thermal evaporation of an Al layer, followed by a post annealing step at 110 °C for 10 h. The semiconducting polymer F8T2 (Sumitomo Chemicals) was dissolved in anhydrous xylene ($5-7 \text{ g L}^{-1}$), spun at 2000 rpm for 1 min in N_2 atmosphere, and annealed at 80 °C for 20 min on a hot plate. C-PMMA dielectric layer²⁵ was deposited on top by spin-coating a 20 g L^{-1} *n*-butyl acetate solution in ambient air at 4000 rpm followed by annealing at 80 °C for 30 min. 1,6-Bis(trichlorosilyl)hexane (Acro Organics) was added to the PMMA (Sigma-Aldrich, $M_w = 120,000$) solution as a cross-linking agent. To realize printed electrodes and interconnects at upper levels of the device we used a silver complex base ink (TEC-IJ-010 InkTec Co., Ltd.), filtered with a 0.2 μm PTFE filter. For the printing steps a custom inkjet printer equipped with a single nozzle drop-on-demand (DOD) piezoelectric head (MicroFab Technologies, Inc.) with orifice diameter 20–30 μm was used. The SEM images were taken with a Hitachi tabletop micro-

scope TM-1000 in charge-up reduction mode. SAP electrodes and TIPS-p FETs-yield measurements were performed in air on arrays of 72 devices with a PEGASUS S200 semiautomatic prober (Wentworth Laboratories, Inc.) connected to a B1500A (Agilent Technologies, Inc.) semiconductor parameter analyzer (SPA). F8T2 transistors were characterized in a nitrogen atmosphere by means of an Agilent 4155B SPA.

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Supporting Information Available: Additional optical microcopy images, curves, SEM images, and distribution of FETs parameters. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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